**CSCI241 – Homework #4 (Logic Gates)  
Name: Alexander Antoun**

**74LS00 – Quad 2-input NAND Gate**

**Diagram

Description automatically generated**

**Truth Tables:  
 Gate #1**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 1)** | **Input B (Pin 2)** | **Output Y (Pin 3)** |
| **LOW** | **LOW** | **HIGH, 5.14 v** |
| **LOW** | **HIGH** | **HIGH, 5.14 v** |
| **HIGH** | **LOW** | **HIGH, 5.14 v** |
| **HIGH** | **HIGH** | **LOW, 0 v** |

**Gate #2**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 4)** | **Input B (Pin 5)** | **Output Y (Pin 6)** |
| **LOW** | **LOW** | **HIGH, 5.14 v** |
| **LOW** | **HIGH** | **HIGH, 5.14 v** |
| **HIGH** | **LOW** | **HIGH, 5.14 v** |
| **HIGH** | **HIGH** | **LOW, 0 v** |

**Gate #3**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 10)** | **Input B (Pin 9)** | **Output Y (Pin 8)** |
| **LOW** | **LOW** | **HIGH, 5.14 v** |
| **LOW** | **HIGH** | **HIGH, 5.14 v** |
| **HIGH** | **LOW** | **HIGH, 5.14 v** |
| **HIGH** | **HIGH** | **LOW, 0 v** |

**Gate #4**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 13)** | **Input B (Pin 12)** | **Output Y (Pin 11)** |
| **LOW** | **LOW** | **HIGH, 5.14 v** |
| **LOW** | **HIGH** | **HIGH, 5.14 v** |
| **HIGH** | **LOW** | **HIGH, 5.14 v** |
| **HIGH** | **HIGH** | **LOW, 0 v** |

**74LS02 – Quad 2-input NOR Gate**

Diagram

Description automatically generated

**Truth Tables:**

**Gate #1**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 2)** | **Input B (Pin 3)** | **Output Y (Pin 1)** |
| **LOW** | **LOW** | **HIGH, 5.11 v** |
| **LOW** | **HIGH** | **LOW, 0 v** |
| **HIGH** | **LOW** | **LOW, 0 v** |
| **HIGH** | **HIGH** | **LOW, 0 v** |

**Gate #2**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 5)** | **Input B (Pin 6)** | **Output Y (Pin 4)** |
| **LOW** | **LOW** | **HIGH, 5.11 v** |
| **LOW** | **HIGH** | **LOW, 0 v** |
| **HIGH** | **LOW** | **LOW, 0 v** |
| **HIGH** | **HIGH** | **LOW, 0 v** |

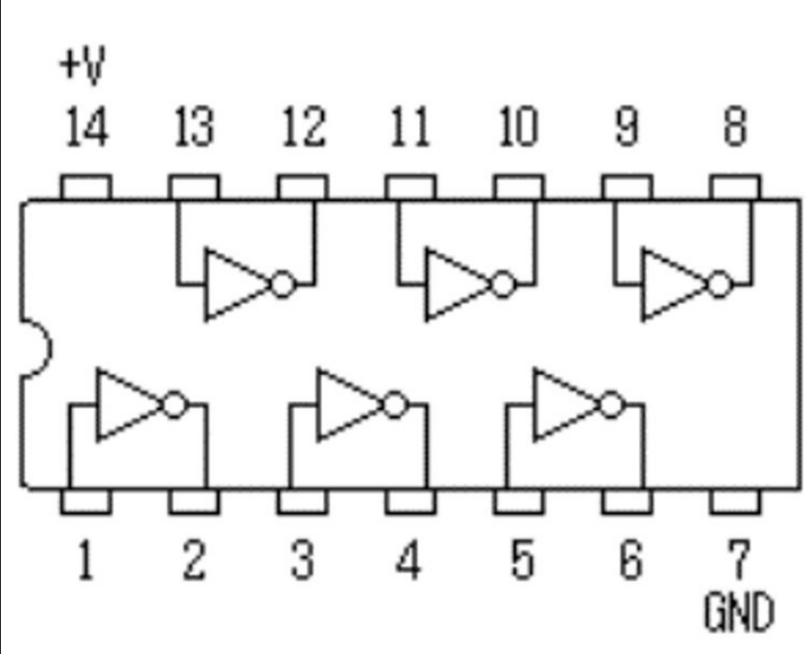
**Gate #3**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 9)** | **Input B (Pin 8)** | **Output Y (Pin 10)** |
| **LOW** | **LOW** | **HIGH, 5.11 v** |
| **LOW** | **HIGH** | **LOW, 0 v** |
| **HIGH** | **LOW** | **LOW, 0 v** |
| **HIGH** | **HIGH** | **LOW, 0 v** |

**Gate #4**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 12)** | **Input B (Pin 11)** | **Output Y (Pin 13)** |
| **LOW** | **LOW** | **HIGH, 5.11 v** |
| **LOW** | **HIGH** | **LOW, 0 v** |
| **HIGH** | **LOW** | **LOW, 0 v** |
| **HIGH** | **HIGH** | **LOW, 0 v** |

**74LS04 – Hex Inverters**

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**Truth Tables:**

**Gate #1**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 1)** | **N/A** | **Output Y (Pin 2)** |
| **LOW** | **N/A** | **HIGH, 5.06 v** |
| **HIGH** | **N/A** | **LOW, 0 v** |

**Gate #2**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 3)** | **N/A** | **Output Y (Pin 4)** |
| **LOW** | **N/A** | **HIGH, 5.06 v** |
| **HIGH** | **N/A** | **LOW, 0 v** |

**Gate #3**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 5)** | **N/A** | **Output Y (Pin 6)** |
| **LOW** | **N/A** | **HIGH, 5.06 v** |
| **HIGH** | **N/A** | **LOW, 0 v** |

**Gate #4**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 9)** | **N/A** | **Output Y (Pin 8)** |
| **LOW** | **N/A** | **HIGH, 5.06 v** |
| **HIGH** | **N/A** | **LOW, 0 v** |

**Gate #5**

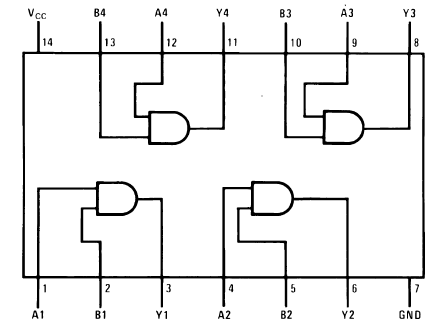
|  |  |  |
| --- | --- | --- |
| **Input A (Pin 11)** | **N/A** | **Output Y (Pin 10)** |
| **LOW** | **N/A** | **HIGH, 5.06 v** |
| **HIGH** | **N/A** | **LOW, 0 v** |

**Gate #6**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 13)** | **N/A** | **Output Y (Pin 12)** |
| **LOW** | **N/A** | **HIGH, 5.06 v** |
| **HIGH** | **N/A** | **LOW, 0 v** |

**74LS08 – Quad 2-input AND Gate**

**Pin Layout:**



**Truth Tables:**

**Gate #1**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 1)** | **Input B (Pin 2)** | **Output Y (Pin 3)** |
| **LOW** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **LOW, 0.00 v** |
| **HIGH** | **LOW** | **LOW, 0.00 v** |
| **HIGH** | **HIGH** | **HIGH, 4.98 v** |

**Gate #2**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 4)** | **Input B (Pin 5)** | **Output Y (Pin 6)** |
| **LOW** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **LOW, 0.00 v** |
| **HIGH** | **LOW** | **LOW, 0.00 v** |
| **HIGH** | **HIGH** | **HIGH, 4.98 v** |

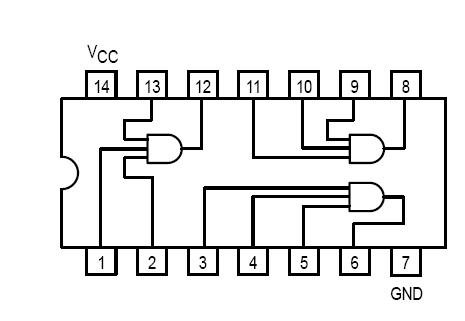
**Gate #3**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 9)** | **Input B (Pin 10)** | **Output Y (Pin 8)** |
| **LOW** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **LOW, 0.00 v** |
| **HIGH** | **LOW** | **LOW, 0.00 v** |
| **HIGH** | **HIGH** | **HIGH, 4.98 v** |

**Gate #4**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 12)** | **Input B (Pin 13)** | **Output Y (Pin 11)** |
| **LOW** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **LOW, 0.00 v** |
| **HIGH** | **LOW** | **LOW, 0.00 v** |
| **HIGH** | **HIGH** | **HIGH, 4.98 v** |

**74LS11 – Triple 3-input AND Gate**

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**Truth Tables:**

**Gate #1**

|  |  |  |  |
| --- | --- | --- | --- |
| **Input A (Pin 1)** | **Input B (Pin 2)** | **Input C (Pin 13)** | **Output Y (Pin 12)** |
| **LOW** | **LOW** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **LOW** | **HIGH** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **HIGH** | **LOW, 0.00 v** |
| **HIGH** | **LOW** | **LOW** | **LOW, 0.00 v** |
| **HIGH** | **LOW** | **HIGH** | **LOW, 0.00 v** |
| **HIGH** | **HIGH** | **LOW** | **LOW, 0.00 v** |
| **HIGH** | **HIGH** | **HIGH** | **HIGH, 5.12 v** |

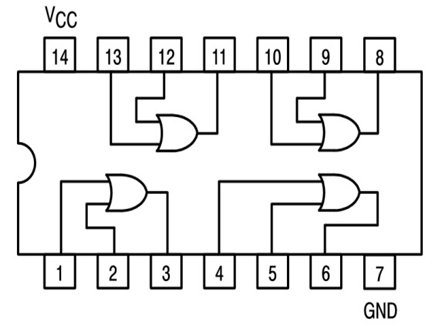
**Gate #2**

|  |  |  |  |
| --- | --- | --- | --- |
| **Input A (Pin 3)** | **Input B (Pin 4)** | **Input C (Pin 5)** | **Output Y (Pin 6)** |
| **LOW** | **LOW** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **LOW** | **HIGH** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **HIGH** | **LOW, 0.00 v** |
| **HIGH** | **LOW** | **LOW** | **LOW, 0.00 v** |
| **HIGH** | **LOW** | **HIGH** | **LOW, 0.00 v** |
| **HIGH** | **HIGH** | **LOW** | **LOW, 0.00 v** |
| **HIGH** | **HIGH** | **HIGH** | **HIGH, 5.12 v** |

**Gate #3**

|  |  |  |  |
| --- | --- | --- | --- |
| **Input A (Pin 11)** | **Input B (Pin 10)** | **Input C (Pin 9)** | **Output Y (Pin 8)** |
| **LOW** | **LOW** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **LOW** | **HIGH** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **HIGH** | **LOW, 0.00 v** |
| **HIGH** | **LOW** | **LOW** | **LOW, 0.00 v** |
| **HIGH** | **LOW** | **HIGH** | **LOW, 0.00 v** |
| **HIGH** | **HIGH** | **LOW** | **LOW, 0.00 v** |
| **HIGH** | **HIGH** | **HIGH** | **HIGH, 5.12 v** |

**74LS32 – Quad 2-input OR Gate**

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**Truth Tables:**

**Gate #1**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 1)** | **Input B (Pin 2)** | **Output Y (Pin 3)** |
| **LOW** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **HIGH, 5.13 v** |
| **HIGH** | **LOW** | **HIGH, 5.13 v** |
| **HIGH** | **HIGH** | **HIGH, 5.13 v** |

**Gate #2**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 4)** | **Input B (Pin 5)** | **Output Y (Pin 6)** |
| **LOW** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **HIGH, 5.13 v** |
| **HIGH** | **LOW** | **HIGH, 5.13 v** |
| **HIGH** | **HIGH** | **HIGH, 5.13 v** |

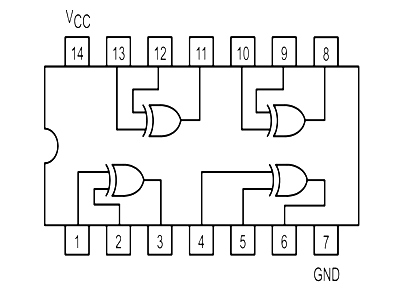
**Gate #3**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 10)** | **Input B (Pin 9)** | **Output Y (Pin 8)** |
| **LOW** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **HIGH, 5.13 v** |
| **HIGH** | **LOW** | **HIGH, 5.13 v** |
| **HIGH** | **HIGH** | **HIGH, 5.13 v** |

**Gate #4**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 13)** | **Input B (Pin 12)** | **Output Y (Pin 11)** |
| **LOW** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **HIGH, 5.13 v** |
| **HIGH** | **LOW** | **HIGH, 5.13 v** |
| **HIGH** | **HIGH** | **HIGH, 5.13 v** |

**74LS86 – Quad 2-input XOR Gate**

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**Truth Tables:**

**Gate #1**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 1)** | **Input B (Pin 2)** | **Output Y (Pin 3)** |
| **LOW** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **HIGH, 5.13 v** |
| **HIGH** | **LOW** | **HIGH, 5.13 v** |
| **HIGH** | **HIGH** | **LOW, 0 v** |

**Gate #2**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 4)** | **Input B (Pin 5)** | **Output Y (Pin 6)** |
| **LOW** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **HIGH, 5.13 v** |
| **HIGH** | **LOW** | **HIGH, 5.13 v** |
| **HIGH** | **HIGH** | **LOW, 0 v** |

**Gate #3**

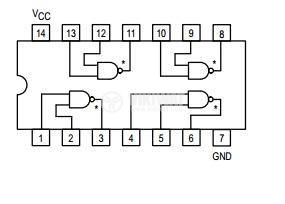
|  |  |  |
| --- | --- | --- |
| **Input A (Pin 10)** | **Input B (Pin 9)** | **Output Y (Pin 8)** |
| **LOW** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **HIGH, 5.13 v** |
| **HIGH** | **LOW** | **HIGH, 5.13 v** |
| **HIGH** | **HIGH** | **LOW, 0 v** |

**Gate #4**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 13)** | **Input B (Pin 12)** | **Output Y (Pin 11)** |
| **LOW** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **HIGH, 5.13 v** |
| **HIGH** | **LOW** | **HIGH, 5.13 v** |
| **HIGH** | **HIGH** | **LOW, 0 v** |

**74LS03 – Quad 2-input NAND Gate with Open Collector Outputs**

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**Truth Tables:**

**Gate #1**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 1)** | **Input B (Pin 2)** | **Output Y (Pin 3)** |
| **LOW** | **LOW** | **INDETERMINATE, 2.7 v** |
| **LOW** | **HIGH** | **INDETERMINATE, 2.7 v** |
| **HIGH** | **LOW** | **INDETERMINATE, 2.7 v** |
| **HIGH** | **HIGH** | **LOW, 0 v** |

**Gate #2**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 4)** | **Input B (Pin 5)** | **Output Y (Pin 6)** |
| **LOW** | **LOW** | **INDETERMINATE, 2.7 v** |
| **LOW** | **HIGH** | **INDETERMINATE, 2.7 v** |
| **HIGH** | **LOW** | **INDETERMINATE, 2.7 v** |
| **HIGH** | **HIGH** | **LOW, 0 v** |

**Gate #3**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 10)** | **Input B (Pin 9)** | **Output Y (Pin 8)** |
| **LOW** | **LOW** | **LOW, 0.00 v** |
| **LOW** | **HIGH** | **HIGH, 5.13 v** |
| **HIGH** | **LOW** | **HIGH, 5.13 v** |
| **HIGH** | **HIGH** | **LOW, 0 v** |

**Gate #4**

|  |  |  |
| --- | --- | --- |
| **Input A (Pin 13)** | **Input B (Pin 12)** | **Output Y (Pin 11)** |
| **LOW** | **LOW** | **INDETERMINATE, 2.7 v** |
| **LOW** | **HIGH** | **INDETERMINATE, 2.7 v** |
| **HIGH** | **LOW** | **INDETERMINATE, 2.7 v** |
| **HIGH** | **HIGH** | **LOW, 0 v** |